# Functional Evaluation for Printed Circuit Board Based on Surface Mount Technology Process Data

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***Abstract*—Functional test strategy adjustment can save testing time and testing costs for companies. Since focusing on testing possible defective products can save a lot of testing time, a natural idea is to evaluate the functionality of the printed circuit boards (PCBs) based on surface mount technology (SMT) process data. Considering the important impact of electrical pathways on PCB functional evaluation, we propose a generative adversarial network method based on circuit layout (CL-GAN). Specifically, the generator is mainly composed of electrical node attribute feature extraction module and electrical connection feature extraction module. These modules are used to model the quality attributes of key nodes in PCB electrical pathways and model electrical connection relationships. The discriminator is trained to perform PCB functional evaluation. Experimental results demonstrate that CL-GAN achieves a 33.34% improvement in F1 score, along with a 96.64% reduction in testing time and a 64.77% decrease of total cost.**

***Keywords- functional test; PCB; generative adversarial network***

## I. INTRODUCTION

Functional test as the last process of printed circuit board (PCB) production, is an important part of the PCB production process. Functional testing simulates the operating environment of the PCB through the test machine, making it work in various design states, so as to check the performance of the PCB under various design states. Through efficient functional testing, PCB defects can be avoided from assembly into electronic devices, thus reducing repair costs.

The fixed test strategy mainly used in factories suffers from the excessive test time and test cost, and it is necessary to be optimized. Typically, fixed test strategies categorize functional test items into mandatory and optional test items. For mandatory test items, all PCBs must be tested; for optional test items, PCBs will be randomly selected for testing according to a predetermined ratio. For example, a typical laptop manufacturer can off-line a batch of PCBs in a dozen seconds, and each PCB takes about tens of seconds for mandatory tests and a few minutes for optional tests. To prevent PCB stack-up, a large number of test machines (more than $10000 each) must be added to test many PCBs at the same time. So fixed test strategy will result in a significant cost.

Academic research on test strategy adjustment is lacking because the details of functional testing are trade secrets. Our research team cooperate with a laptop manufacturer to complete the mathematical modeling of the general framework of functional testing for the first time [1], and propose test item selection based on yield prediction [2], functional test cost reduction based on fault tree analysis and binary optimization [3], and other solutions. These solutions achieve the purpose of reducing test time and reducing functional test costs by adjusting the test ratio of the selected test items. However, these solutions require the collection of a large amount of historical functional test data. Therefore, they are only applicable to the case of mass production of PCBs, and the test items of the test machine need to be frequently set according to the selected test items. The PCB production process is highly coupled, and each production step may have an impact on the PCB function. Therefore, a natural idea is to evaluate the PCB function through surface mount technology (SMT) process data, and focus on testing PCBs that may have defects. This method does not require the collection of a large amount of PCB functional test data, nor does it require the modification of the test machine settings, and can save more testing time.

Due to the small number of defective PCBs and the extremely unbalanced ratio between defective and good products, PCB function evaluation mainly relies on anomaly detection technology [4][5]. When existing anomaly detection algorithms are applied to our problem, they usually analyze the relationship between attributes from PCB process data and ignore the electrical pathways of the PCB, making it difficult to detect potential electrical faults, and thus the evaluation of PCB functions may be inaccurate. Since the realization of PCB functions depends on electronic components and corresponding electrical pathways, any electrical faults may cause PCB functional defects. Therefore, electrical pathways have an important impact on PCB functional evaluation.



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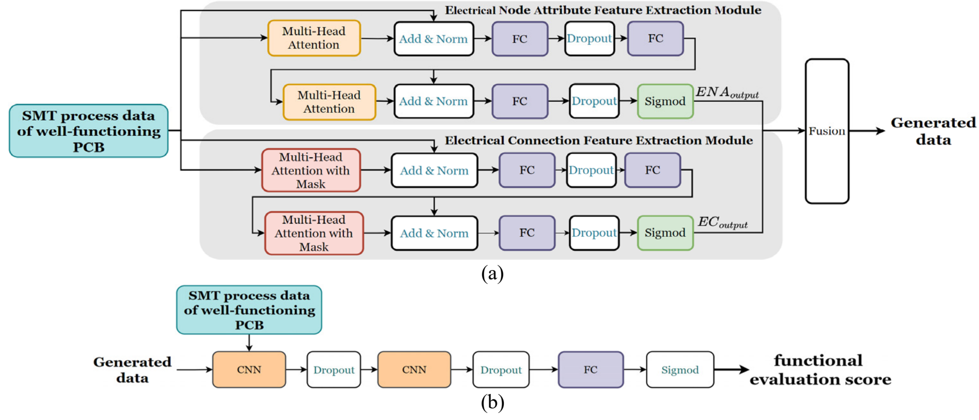


Figure 1. (a) Generator structure of CL-GAN. (b) Discriminator structure of CL-GAN

To model the electrical pathways, we propose a GAN method based on circuit layout: CL-GAN, which is used to evaluate the PCB function. GAN can be used to model the production data distribution of well-functioning PCBs, thereby effectively identifying outliers about this data distribution—defective PCBs. First, we design two modules in the generator part. The electrical node attribute feature extraction module is used to extract the features between the quality attributes of the key nodes in the PCB electrical pathways. For the electrical connection feature extraction module, we design a mask mechanism that reflects the electrical connection relationship based on the PCB circuit layout, so that the model can model the circuit structure of the PCB. Then, we fuse the outputs of the two modules to ensure that the generated data is more realistic. Next, we train the discriminator. Finally, the trained discriminator is used to evaluate the PCB function, achieving an accuracy of 97.99% and an F1 score of 0.6667. Compared with the cooperative factory approach, we can save 96.64% of testing time and 64.77% of total cost.

The main contributions of this paper are:

- To model electrical pathways, we propose CL-GAN. The two modules of the generator extract electrical node attribute features and electrical connection features respectively. Our method achieves the best results after experimental verification.
- To model the electrical connection relationships, we propose a mask mechanism based on the PCB circuit layout. This mechanism can reflect the actual electrical connection relationships, allowing the model to accurately model the circuit structure of the PCB.
- To model the quality attributes of key nodes in PCB electrical pathways, we design an electrical node attribute feature extraction module, which can effectively capture the association between quality attributes and electrical functions.

## II. Method

The overall architecture of CL-GAN is shown in Figure 1. Due to the effectiveness of multi-head attention in capturing long-range dependencies and outstanding performance, we use multi-head attention as the core component to design CL-GAN.

### A. *Electrical Node Attribute Feature Extraction Module*

In order to better model the quality attributes of key nodes in PCB electrical pathways, we design an electrical node attribute feature extraction module. This module uses Transformer to extract attribute features of electrical nodes. With its powerful attention mechanism, it can effectively capture the complex relationship between various attributes in the data. The calculation process of the multi-head attention mechanism can be expressed as:

$$Q, K, V = XW_Q, XW_K, XW_V \tag{1}$$

$$\text{Attention} = \text{softmax}\left(\frac{QK^T}{\sqrt{d_k}}\right)V \tag{2}$$

$$head_h = \text{Attention}(Q_h, K_h, V_h) \tag{3}$$

$$\text{MultiHead}(X) = \text{Concat}(head_1, \dots head_h)W_o \tag{4}$$

where $W_Q, W_K, W_V, W_O$ are learnable parameters, Q is the query matrix, K is the key matrix, V is the value matrix, and $\sqrt{d_k}$ is the scaling factor.

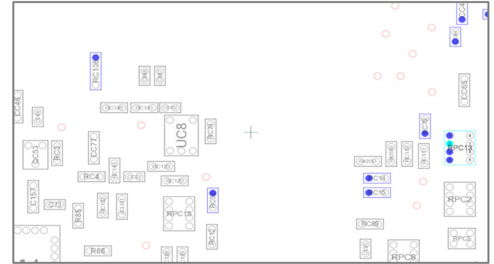

Figure 2. Part of PCB circuit layout. When the pin is clicked, it turns blue, and the pins connected by the circuit turn purple.

### B. *Electrical Connection Feature Extraction Module*

When modeling the electrical connection relationship of PCB, directly using the multi-head attention mechanism may fail to capture the complex component interconnection relationships in the circuit, making it impossible to model the actual circuit structure. Therefore, we design a mask mechanism that reflects the electrical connection relationship based on the circuit layout



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that reflects the node position and circuit structure. Part of PCB circuit layout is shown in Figure 2. This mechanism highlights the circuit structure by shielding the attention calculation between nodes that do not have circuit connections, ensuring that the model can accurately model the circuit structure when processing data, focusing on the electrical connection relationship between nodes. Specifically, we obtain the circuit structure of the PCB based on the circuit layout. Then, based on the circuit structure, we retain the attention between nodes that have circuit connections. In this way, nodes that have attention connections with each other are circuit connected and have actual physical meanings. The mask matrix $A$ can be obtained from the following formula:

$$A_{ij} = \begin{cases} 1 & (i,j) \in \mathbb{K} \\ 0 & \text{others} \end{cases} \tag{5}$$

where $i, j$ refer to solder joint $i, j$, $\mathbb{K}$ is a set storing pairs of solder joints that are circuit-connected.

At this point, to calculate attention, equation (2) should be redefined as:

$$\text{Attention} = \text{softmax}\left(\frac{QK^T}{\sqrt{d_k}}\right)V \odot A \tag{6}$$

The electrical connection relationship can be reflected by using masks designed based on circuit layout. Such masks provide a clue for the model to guide it to focus on the truly important circuit structure, thereby improving the model's ability to understand PCB process data. Moreover, the introduction of the mask mechanism also reduces computing resources and effectively reduces the amount of information that the model needs to process, which not only shortens the training time, but also reduces memory usage and improves operating efficiency.

### C. *Fusion Module*

Fusing the outputs of the two modules allows the generator to not only capture the complex relationships between the various attributes of the process data, but also model the circuit structure of the PCB. This significantly improves the authenticity of the generated data. The output $\text{FS}_{\text{output}}$ of the fusion module is as follows:

$$\text{FS}_{\text{output}} = \alpha \cdot \text{ENA}_{\text{output}} + \beta \cdot \text{EC}_{\text{output}} \tag{7}$$

where $\text{ENA}_{\text{output}}$ represents the output of the electrical node attribute feature extraction module, $\text{EC}_{\text{output}}$ represents the output of the electrical connection feature extraction module, $\alpha$ and $\beta$ are hyperparameters.

### D. *Discriminator Structure*

The discriminator structure is shown in Figure 1.b, which is mainly composed of CNN. The convolution layer is responsible for extracting local features. This enables the discriminator to effectively capture the multi-level features of the input data and extract subtle differences. After being processed by the Sigmod, the functional evaluation score is output to effectively distinguish between real samples and fake samples. As the training process proceeds, the generator continuously adjusts parameters to generate data that is closer to reality, while the discriminator continuously improves its discrimination ability.

During the function evaluation process, the discriminator will give higher scores to well-functioning PCB data that often appear during the training process; while for unseen PCB defective data, because its features are quite different from the well-functioning data in the training set, the discriminator will give lower scores when dealing with such data, thereby achieving PCB function evaluation.

### E. *Loss Function*

The loss functions for the generator and discriminator are as follows:

$$\text{BCE}(y, \hat{y}) = -\frac{1}{N}\sum_{i=1}^{N}(y_i \log(\hat{y}_i) + (1 - y_i)\log(1 - \hat{y}_i)) \tag{8}$$

$$L_D = \text{BCE}(y, D(x)) + \text{BCE}\left(\tilde{y}, D\big(G(x)\big)\right) \tag{9}$$

$$L_G = \text{BCE}\left(y, D\big(G(x)\big)\right) \tag{10}$$

where $\text{BCE}(y, \hat{y})$ is a binary cross entropy loss function that measures the difference between the predicted value $\hat{y}$ and the actual value $y$, $x$ represents the input data, $y = 1$ denotes the corresponding labels, $\tilde{y} = 0$ indicates the labels of the generated data, $D(x)$ represents the output of the discriminator with x as input, $G(x)$ represents the generated data of the generator with x as input, $L_D$ represents the loss of the discriminator, and $L_G$ represents the loss of the generator.

### F. *Functional Evaluation*

We employ the trained discriminator for function evaluation. Specifically, the production process data of a PCB is input into the trained discriminator to obtain a functional evaluation score. Subsequently, a threshold $\delta$ is established, and the PCB function evaluation result can be derived from the following formula:

$$Result = \begin{cases} 0, & \text{functional evaluation score} \geq \delta \\ 1, & \text{functional evaluation score} < \delta \end{cases} \tag{11}$$

where $Result = 0$ indicates that the PCB is evaluated as a good product, while $Result = 1$ signifies that the PCB is assessed as a defective product.

## III. EXPERIMENTS

To validate the performance of proposed CL-GAN, we conduct experiments using real PCB data collected from a cooperating factory's automated production line, specifically from the solder paste inspection and functional testing machines. According to expert knowledge, solder paste printing has a significant impact on the functionality and reliability of PCBs. Therefore, we use the core solder paste inspection data to conduct functional evaluation. The data collection period span one week, during which a total of 449 PCBs with optional test items are collected. Among these, 445 PCBs exhibit satisfactory functionality, while 4 are identified as defective.



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### A. *Data preprocessing and evaluation metrics*

We select 300 well-functioning PCB data as the training set and the rest as the test set. Each data is normalized by column. The dimension of each data is [3152, 9], where 3152 represents the number of solder joints on a PCB and 9 refers to the number of attributes of each solder joint. To evaluate the performance of CL-GAN, we use two widely recognized indicators: accuracy and F1 score. Based on the formula for computational cost provided by [1], we propose a formula for computational cost difference $\Delta C$, as shown below:

$$\Delta C = N \cdot C_T - (n \cdot C_T + \Delta C_R \cdot k) \quad (12)$$

This formula indicates the cost that our proposed solution can save compared with the original solution. N refers to the number of PCBs in the test set, $C_T$ is the cost of testing a PCB with optional items, n refers to the number of PCBs that need to be tested after functional evaluation, $\Delta C_R$ refers to the cost difference between repairing a faulty PCB as a finished laptop and repairing it as a PCB, and k refers to the number of defective PCBs that are missed by our solution.

### B. *Experimental Results*

Our proposed CL-GAN is compared with One-Class SVM [6], REPEN [7], DIF [8], SLAD [9] and a conventional GAN [10] composed of a three-layer fully connected network. The experimental results are shown in table 1. Although the conventional GAN has a simple model structure, it performs better than One-Class SVM under imbalanced conditions, demonstrating GAN's ability to effectively capture underlying patterns in data. REPEN, DIF, and SLAD are anomaly detection methods specifically designed for tabular data. However, due to their neglect of the electrical pathways in PCBs, their detection performance is suboptimal.

Additionally, the results show that CL-GAN achieve excellent detection performance on the real PCB dataset, with the best accuracy and F1 score. This is because CL-GAN's various components efficiently extract electrical pathways features, leading to more diverse and realistic sample generation. This is a key reason for its superiority over other methods on imbalanced datasets.

Our method determines that 5 PCBs needed to be tested. Compared with the cooperative factory that needs to test 149 PCBs, we can save 96.64% of the testing time. At the same time, since 3 of the 5 PCBs are actually defective, one defective PCB was missed. Therefore n=5, k=1. Based on the relevant data in [1] and [3], we calculate that $C_T$ is 0.4 and $\Delta C_R$ is 19. Then we can calculate $\Delta C = 38.6$ , which means 64.77% cost saving.

TABLE I. Result of Experiments

| Model | Accuracy | F1 |
|---|---|---|
| **One-class SVM** | 0.7114 | 0.1224 |
| **REPEN** | 0.9128 | 0.3158 |
| **DIF** | 0.9530 | 0.4615 |
| **SLAD** | 0.9732 | 0.5 |
| **GAN** | 0.8725 | 0.24 |
| **CL-GAN** | **0.9799** | **0.6667** |

## IV. CONCLUSION

In this paper, we propose a GAN method based on circuit layout: CL-GAN for PCB functional evaluation.

(1) To model the electrical connection relationships, we propose a mask mechanism based on circuit layout that reflects the PCB electrical connection relationships. The generator of our model is mainly composed of an electrical node attribute feature extraction module and an electrical connection feature extraction module, which makes the generated data more realistic, thereby guiding the discriminator to better improve its identification ability and achieve accurate functional evaluation.

(2) Experimental results show that our model achieves a 33.34% improvement in F1 score. Moreover, CL-GAN can save 96.64% of testing time and 64.77% of the total cost, providing an important reference for the factory we cooperate with to adjust the PCB functional test strategy.

In the future, we will also collect more PCB process data of different models to further improve our algorithm and obtain better results.

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